



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

11.7

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/828,546

04/19/2004

Kern W. Wong

P05310C1

3883

23990

7590

03/26/2007

DOCKET CLERK

P.O. DRAWER 800889

DALLAS, TX 75380

EXAMINER

LAXTON, GARY L

ART UNIT

PAPER NUMBER

2838

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
--	-----------	---------------

3 MONTHS

03/26/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

10/828,546

Applicant(s)

WONG ET AL.

Examiner

Gary L. Laxton

Art Unit

2838

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 23,24 and 27-48 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 23,24,27,38,39,41,42 and 46 is/are allowed.
- 6) ☒ Claim(s) 28,29,32,40,43-45,47 and 48 is/are rejected.
- 7) ☒ Claim(s) 30,31 and 33-37 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments with respect to claims 28, 29, 32, 40, 43, 44, 45, 47 and 48 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 44 and 48 rejected under 35 U.S.C. 102(e) as being anticipated by  
Guenot et al (US 6,529,066).

Guenot et al. disclose a band-gap reference circuit, comprising: a current source (6B) for generating a current; a circuit branch comprising a resistor connected in series with a first base-emitter diode (R1, 8B), wherein the current from the current source develops a combined voltage across the resistor and the first base-emitter diode; a second base-emitter diode (8A); an adjustment circuit (12) for adjusting a band-gap reference voltage based on the combined voltage and a base-emitter voltage of the second base-emitter diode; and a correction circuit (32) coupled

Art Unit: 2838

to the adjustment circuit and cooperable with the adjustment circuit for at least “partially” offsetting a drop-off in the band-gap reference voltage caused by the second base-emitter diode (e.g. Guenot et al. disclose a band-gap reference circuit, comprising: a current source for generating a current; a circuit branch comprising a resistor connected in series with a first base-emitter diode, wherein the current from the current source develops a combined voltage across the resistor and the first base-emitter diode; a second base-emitter diode; an adjustment circuit for adjusting a band-gap reference voltage based on the combined voltage and a base-emitter voltage of the second base-emitter diode; and a correction circuit coupled to the adjustment circuit and cooperable with the adjustment circuit for at least “partially” offsetting a drop-off in the band-gap reference voltage caused by the second base-emitter diode (e.g. Vboost).

4. Claims 44 and 48 are rejected under 35 U.S.C. 102(b) as being anticipated by Opris (US 6,121,824).

Opris discloses a band-gap reference circuit, comprising: a current source (I) for generating a current; a circuit branch comprising a resistor connected in series with a first base-emitter diode (R1, Q<sub>L</sub>), wherein the current from the current source (I) develops a combined voltage across the resistor and the first base-emitter diode; a second base-emitter diode (Q1); an adjustment circuit (A1) for adjusting a band-gap reference voltage based on the combined voltage and a base-emitter voltage of the second base-emitter diode; and a correction circuit coupled to the adjustment circuit and cooperable with the adjustment circuit for at least “partially” offsetting a drop-off in the band-gap reference voltage caused by the second base-emitter diode (fig. 2).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 28, 29, 32, 40, 43 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guenot et al. in view of Marty.

Guenot et al. discloses a bandgap reference circuit having a current source (6A, 6B or 6C); a circuit branch(s) (6A & 6B) with positive and negative temperature coefficients as claimed; further base emitter diode (8A) adjustment circuit (32 & Vboost) for “partially offsetting the voltage drop from (8A).

However, Guenot et al. does not disclose a startup circuit.

Marty a regulator circuit including a startup circuit (20) connected to the output of an adjustment circuit (5) for ensuring proper startup of the regulator circuit.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Guenot et al. to include a startup circuit to ensure the proper startup of the circuit as taught by Marty.

7. Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Guenot et al. in view of May.

Guenot et al. discloses a bandgap reference circuit having a current source (6A, 6B or 6C); a circuit branch(s) (6A & 6B) with positive and negative temperature coefficients as